II. REMARKS

Claims 27-38 are pending. Claims 27, 30, 31, and 35 have been amended, and claims 37-38 have been newly added. Attached hereto is Appendix A showing the changes made to the amended claims and the specification. Reconsideration is respectfully requested.

1. Objection to Drawings

The drawings were objected to because the reference character 96 was used to designate both a source and a source line on page 12 of the specification. Page 12 of the specification has been amended to correct this informality. The recitation of source and source line 96 should have been conductive block 54 and conductive layer 52, as shown in Fig. 2N. Applicants submit no new matter is added. Approval of the specification amendment and withdrawal of this objection are respectfully requested.

2. Objection to Title

The title was objected to for not being descriptive, presumably because the method claims have been withdrawn from this case in response to a restriction requirement. The title has been amended to be clearly indicative of the invention to which the claims are directed. Approval of the title is respectfully requested.

3. Rejection of Claims 27-36 Under § 112

Claims 27-36 were rejected under 35 U.S.C. 112 second paragraph as being indefinite for failing to provide adequate antecedent basis.

Claims 27 and 31 have been amended to more clearly recite that it is the first and second regions that are of a second conductivity type. Claim 31 has been amended to delete the claim language "said substrate including over the channel regions", which was objected to by the Examiner.

The Applicants respectfully traverse the Examiner's position that "each of the source regions" in line 1 of claim 34 lacks sufficient antecedent basis. Claim 34 depends upon claim 31, which recites a plurality of memory cell pairs, where each memory cell pair includes a source

region. Thus, there are a plurality of the source regions in the array of memory devices, and making a reference to "each" of those source regions is proper. It is therefore submitted that there is proper antecedent basis for the term "each of the source regions".

4. Rejection of Claims 27-30 Under § 102(b)

Claims 27-30 were rejected under 35 U.S.C. 102(b) as being anticipated by USP 5,939,749 (Taketa).

The present invention is a memory cell architecture that facilitates the voltage coupling between the source region 50 and the floating gate 14, while still providing a small source region for smaller cell geometries. The improved voltage coupling is accomplished by providing a conductive block 54 that is electrically connected to the source region 50, where the conductive block 54 includes a lower portion 60 disposed adjacent to and insulated from one end of the floating gate 14, and an upper portion 62 disposed over and insulated from a portion of the floating gate 14, as shown in Figure 2N of the present application. The proximity of the lower and upper portions of the conductive block 54 to the floating gate 14 provides for enhanced voltage coupling therebetween.

The control gate 68 is disposed adjacent to the other end of the floating gate 14 for Fowler Nordheim tunneling. The control gate includes a first portion 70 disposed adjacent to and insulated from the floating gate 14, and a second portion 72 disposed over and insulated from the floating gate. The conductive block and control gate overlap different portions of the floating gate so the control gate does not interfere with the voltage coupling with the conductive block 54, and the conductive block 54 does not interfere with the Fowler Nordheim tunneling to the control gate 68.

In contrast, Taketa teaches a cell design using a source electrode 14 in electrical contact with the source region 3 to reduce the resistance of the source lines, where the source electrode 14 extends up and over both the floating gate 32 and the control gate 9 (see Figs. 1 and 6, and Col. 10, lines 15-22). Having the control gate disposed between the upper portion of the source electrode and the floating gate prevents the desired voltage coupling therebetween that is the featured benefit of the present invention.

Claim 27 as amended recites that the floating gate consists of first and second portions integrally formed together, where the conductive source region upper portion is disposed over and insulated from the floating gate first portion *and not the floating gate second portion*, and the control gate second portion is disposed over and insulated from the floating gate second portion *and not the floating gate first portion*. In contrast, Taketa teaches that the control gate is disposed over part (see Fig. 6) or all (see Fig. 1) of the floating gate 32, and the upper portion of the source electrode 14 is disposed over both the control gate 9 and the floating gate 32. Thus, the desired enhanced voltage coupling between the source electrode and floating gate is prevented. Therefore, it submitted that Taketa does not anticipate amended claim 27 (and claims 28-30 dependent thereon).

5. Rejection of Claims 31-36 Under § 103(a)

Claims 31-36 were rejected under 35 U.S.C. 103(a) as being unpatentable over Taketa in view of USP 6,211,547 (Kao).

Claim 31 has also been amended in a similar manner as was claim 27, and now recites that each of the memory cell pairs includes a pair of the floating gates (each consisting of a first portion and a second portion integrally formed together), where the electrically conductive source region upper portion is disposed over and insulated from the floating gate first portions *and not the floating gate second portions*, and each of the pair of electrically conductive control gates are adjacent one of the floating gates and each has a second portion disposed over and insulated from the second portion *and not the first portion* of the one floating gate. For the reasons set forth above in Part 4, it is respectfully submitted that Taketa fails to teach or suggest the memory device array as recited in claim 31. Furthermore, it is submitted that the addition of Kao fails to remedy the deficiencies of the Taketa reference.

It is therefore submitted that claim 31, along with claims 32-36 dependent thereon, are allowable over the combination of Taketa and Kao references.

6. New Claims

Claims 37 and 38 have been newly added. These claims recite insulation material disposed between the source region second portion and the floating gate first portion which has a thickness for permitting voltage coupling therebetween. Applicants respectfully submit that no new matter has been added, and that these claims are allowable over the references relied up by the Examiner. Specifically, there is no apparent voltage coupling between the upper portion of the source electrode 14 and the floating gate 32 of the Taketa device, especially in light of the fact that the control gate 9 is disposed therebetween.

Allowance of the newly added claims is respectfully requested.

For the foregoing reasons, it is respectfully submitted that the claims are in an allowable form, and action to that end is respectfully requested.

Respectfully submitted,

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APPENDIX A: MARKINGS TO SHOW CHANGES MADE

Changes Made To Paragraph On Page 12, Lines 4 to 24 In The Specification:

As shown in Fig. 2N, first and second regions 50/80 form the source and drain for each cell (those skilled in the art know that source and drain can be switched during operation). The channel region 92 for each cell is the portion of the substrate that is in-between the source and drain 50/80. Poly blocks 68 constitute the control gate, and poly layer 14 constitutes the floating gate. Oxide layers 32, 36, 46 and 48 together form an insulation layer that is disposed adjacent to and over floating gate 14, to isolate it from [source 96] conductive block 54 and conductive layer 52. Oxide layers 36 and 64 together form an insulation layer that isolates the [source lines 96] conductive block 54 and conductive layer 52 from the control gates 68. The control gates 68 have one side aligned to the edge of the second region 80, and are disposed over part of the channel regions 92. Control gates 68 have lower portions 70 that are disposed adjacent to the floating gates 14 (insulated therefrom by oxide layer 64), and upper protruding portions 72 that are disposed (extend) over a portion of adjacent poly layers 14 (insulated therefrom by oxide layers 64). A notch 94 is formed by the protruding portion 72, where the sharp edge 66 of floating gate 14 extends into the notch 94. Each floating gate 14 is disposed over part of the channel region 92, is partially overlapped at one end by the control gate 68, and partially overlaps the first region 50 with its other end. Conductive blocks 54 and the conductive layers 52/56 together form source lines 96 that extend across the columns of memory cells. Upper portions 62 of source lines 96 extend over but are insulated from the floating gates 14, while lower portions 60 of source lines 96 are adjacent to but insulated from floating gates 14. As illustrated in the Fig. 2N, the process of the present invention forms pairs of memory cells that mirror each other. The pairs of mirrored memory cells are insulated from other cell pairs by oxide layer 76, nitride spacers 78 and BPSG 86.

Changes to Claims

27. (Amended) An electrically programmable and erasable memory device comprising:

a substrate of semiconductor material of a first conductivity type;

first and second spaced-apart regions [in the substrate] of a second conductivity type formed in the substrate, with a channel region therebetween;

[a first insulation layer disposed over said substrate;]

an electrically conductive floating gate disposed over [said first insulation layer and extending over] and insulated from a portion of said channel region and [over] a portion of the first region, wherein the floating gate consists of a first portion and a second portion integrally formed together; [and]

an electrically conductive source region disposed over and electrically connected to the first region in the substrate, the source region having a lower portion that is disposed adjacent to and insulated from the floating gate and an upper portion that is disposed over and insulated from the floating gate first portion and not the floating gate second portion; and

an electrically conductive control gate having a first portion and a second portion, the first control gate portion being disposed adjacent to and insulated from the floating gate, and the second control gate portion being disposed over and insulated from the floating gate second portion and not the floating gate first portion.

30. (Amended) The device of claim 27, further comprising:

an [second] insulation layer disposed [over and adjacent] between the floating gate and the control gate, and having a thickness permitting Fowler-Nordheim tunneling of charges therethrough[; and

an electrically conductive control gate having a first portion and a second portion, the first control gate portion being disposed adjacent to the second insulation layer and the floating gate, and the second control gate portion being disposed over a portion of the second insulation layer and a portion of the floating gate].

31. (Amended) An array of electrically programmable and erasable memory devices comprising:

a substrate of semiconductor material of a first conductivity type;

spaced apart isolation regions formed on the substrate which are substantially parallel to one another and extend in a first direction, with an active region between each pair of adjacent isolation regions; and

each of the active regions including a column of pairs of memory cells extending in the first direction, each of the memory cell pairs including:

a first region and a pair of second regions spaced apart in the substrate and having a second conductivity type, with channel regions formed in the substrate between the first region and the second regions,

[a first insulation layer disposed over said substrate including over the channel regions,]

a pair of electrically conductive floating gates each disposed over [the first insulation layer and extending over] and insulated from a portion of one of the channel regions and [over] a portion of the first region, wherein each of the floating gates consists of a first portion and a second portion integrally formed together, [and]

an electrically conductive source region disposed over and electrically connected to the first region in the substrate, the source region having a lower portion that is disposed adjacent to and insulated from the pair of floating gates and an upper portion that is disposed over and insulated from the [pair of] floating gate[s] first portions and not the floating gate second portions; and

a pair of electrically conductive control gates each having a first portion and a second portion, wherein for each of the control gates, the first control gate portion is disposed adjacent to and insulated from one of the floating gates and the second control gate portion is disposed over and insulated from the second portion and not the first portion of the one floating gate.

35. (Amended) The device of claim 31, wherein each of the memory cell pairs further comprises:

an [second] insulation layer disposed [over and adjacent to] between each of the floating gates and each of the control gates and having a thickness permitting Fowler-Nordheim tunneling of charges therethrough[; and

a pair of electrically conductive control gates each having a first portion and a second portion, the first control gate portion being disposed adjacent to the second insulation layer and one of the floating gates, and the second control gate portion being disposed over a portion of the second insulation layer and a portion of the one floating gate].